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POST THERMAL TREATMENT METHODS OF FORMING HIGH DIELECTRIC LAYERS OVER INTERFACIAL LAYERS IN INTEGRATED CIRCUIT DEVICES

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority to Korean Patent Application No. 2002-54606, filed on September 10, 2002 in the Korean Intellectual Property Office, Korean Patent Application No. 2003-61702 filed on September 4, 2003 in the Korean Intellectual Property Office, and CONTINUATION-IN-PART United States Patent Application No. 10/650,415, filed on August 28, 2003, the NOW U.S. PAT. NO. 6,875,678 disclosures of which are incorporated herein in their entirety by reference.

FIELD OF THE INVENTION

[0002] The present invention relates to methods for forming dielectric layer structures in integrated circuit devices.

BACKGROUND OF THE INVENTION

[0003] As semiconductor devices become highly integrated and the thickness of gate insulating layers becomes smaller, new materials are being developed for the gate insulating layers. Silicon oxide (SiO_2) layers may be used as gate insulating layers in today's semiconductor devices. Silicon oxides may be used as gate insulating layers because of their thermal stability, reliability, and ease of production. However, the dielectric constant of silicon oxide layers is about 3.9, which may pose some limitations on the ability to scale silicon oxide layers to different sized semiconductor devices. In particular, the leakage current of silicon oxide can greatly increase as the thickness of the silicon oxide layer decreases.

[0004] As an alternative to silicon oxide layers, high dielectric layers have been studied. High dielectric layers can be used in place of silicon oxide layers as gate insulating layers. When high dielectric layers are used as the gate insulating layer, leakage current can be reduced by making the high dielectric layer thicker than the silicon oxide layer while maintaining the same capacitance value. Some common substances that may be used in the formation of high